WHAT IS CLAIMED IS:

1. A semiconductor memory device operable in a merged data input/output pin (DQ) test mode, comprising:

a first path circuit;

a second path circuit; and

a merged output generator configured to generate a merged data bit having a single data rate (SDR) pattern and/or a dual data rate (DDR) pattern.

2. The semiconductor memory device of claim 1, wherein the merged data bit is generated in response to outputs of the first and second path circuits.

3. The semiconductor memory device of claim 1, further comprising a control signal generator configured to generate a first and second SDR signal and a first and second transmission signal pair.

4. The semiconductor memory device of claim 3, wherein the first and second SDR signals and the first and second transmission signal pairs control the first and second path circuits.

5. The semiconductor memory device of claim 1, wherein the control signal generator comprises:

a first NOR gate receiving first and second output clock signals;

first, second, and third inverters, wherein outputs of the second and

third inverters are the first transmission signal pair;

a second NOR gate receiving third and fourth output clock signals;

fourth, fifth, and sixth inverters, wherein outputs of the fifth and sixth inverts are the second transmission signal pair;

a first NAND gate generating the second SDR signal; and

a second NAND gate generating the first SDR signal.

6. The semiconductor memory device of claim 5, wherein the first SDR signal is generated in response to a main signal of the first transmission signal pair and a complementary signal of the second transmission signal pair.

7. The semiconductor memory device of claim 5, wherein the second SDR signal is generated in response to a complementary signal of the first transmission signal pair and a main signal of the second transmission signal pair.

8. The semiconductor memory device of claim 3, wherein the first path circuit comprises:

a first inverter receiving a merging flag signal;

a NOR gate receiving an output of the first inverter and a first data bit;

a transmission gate transferring an output of the NOR gate in response to the first transmission signal pair;

a PMOS transistor connecting a power supply to the transmission gate

in response to the second SDR signal;

a latch holding a voltage level of an output node of the transmission gate; and

a second inverter converting an output of the latch into an output of the first path circuit.

9. The semiconductor memory device of claim 8, wherein the first data path circuit propagates the first data bit generated at a first edge of a clock signal.

10. The semiconductor memory device of claim 8, wherein the first path circuit further comprises an NMOS transistor resetting the output node of the transmission gate in response to a reset signal.

11. The semiconductor memory device of claim 3, wherein the second path circuit comprises:

a first inverter receiving a merging flag signal;

a NOR gate receiving an output of the first inverter and a second data bit;

a transmission gate transferring an output of the NOR gate in response to the second transmission signal pair;

a PMOS transistor connecting a power supply to the transmission gate in response to the first SDR signal;

a latch holding a voltage level of an output node of the transmission gate; and

a second inverter converting an output of the latch into an output of the second path circuit.

12. The semiconductor memory device of claim 11, wherein the second data path circuit propagates the first data bit generated at a second edge of a clock signal.

13. The semiconductor memory device of claim 11, wherein the second path circuit further comprises an NMOS transistor resetting the output node of the transmission gate in response to a reset signal.

14. The semiconductor memory device of claim 1, wherein the merged output generator comprises;

a NAND gate receiving outputs of the first and second path circuits; and an inverter converting an output of the NAND gate into the merged data bit.

15. The semiconductor memory device of claim 9, wherein the first edge is a rising edge of the clock signal.

16. The semiconductor memory device of claim 12, wherein the second edge is a falling edge of the clock signal.

17. A semiconductor for operating in a merged data input/output pin (DQ) test mode, comprising:

a control signal generator for generating a first and second single data rate (SDR) signal and a first and second transmission signal pair;

a first path circuit for receiving one of the first and second SDR signals and first and second transmission pairs;

a second path circuit for receiving one of the first and second SDR signals and first and second transmission pairs; and

a merged output generator for generating a merged data bit, wherein the merged data bit has an SDR or dual data rate (DDR) pattern.

18. The semiconductor memory device of claim 17, wherein the merged data bit is generated in response to a first and second output signal of the first and second path circuits.